

ABSTRACT OF THE DISCLOSURE

An interconnect trench is formed on a dielectric layer 12 and a first HSQ layer 14 formed on a semiconductor substrate, and
5 a tantalum family barrier metal layer 24a is formed all over the substrate. Then a seed copper-containing metal layer 60 and a plated copper layer 62 are formed so as to fill a part of the interconnect trench. After that, a bias-sputtered copper-containing metal layer 64 is formed on the plated copper
10 layer 62 so as to fill the remaining portion of the interconnect trench and then heat treatment is performed. As a result, a dissimilar metal contained in the bias-sputtered copper-containing metal layer 64 diffuses uniformly into the plated copper layer 62.